REMARKS

In the Official Action mailed on **23 August 2007**, the Examiner reviewed claims 1-26. Claims 1, 13, and 14 were rejected under U.S.C. § 101. Claims 1, 13, 14, and 20 were rejected under 35 U.S.C. § 112. Claims 1, 13, 14, and 20 were objected to. Claims 20-26 were rejected on the ground of non-statutory double patenting over claims 1-20 of USPN 6,480,489. Claims 20-26 were rejected under 35 U.S.C. § 103(a) based on Iyer et al. (US Pub No. 2005/0240745 hereinafter "Iyer"), and Hammond et al. (USPN 5,774,686 hereinafter "Hammond"). Claims 1-19 were rejected under 35 U.S.C. § 102(e) based on Iyer.

Rejections under 35 U.S.C. § 101

Claims 1, 13, and 14 were rejected as directed to non-statutory subject matter. In particular, Examiner avers that the claims do not "include all elements of the invention as described in the abstract in order to provide a concrete, useful and tangible result."

Accordingly, Applicant has amended the abstract to reflect current amendments to the independent claims. The amended abstract closely follows the amended claim as required by MPEP § 608.01(b).

In addition, Applicant has amended claim 1, 13 and 14 to include a "hybrid buffer" as described in the abstract.

Examiner also avers that undue experimentation would be required to understand what completion lines are and hence "the disclosed invention is inoperative and lacks utility." Applicant addresses this rejection in the following section (while addressing a similar rejection under 35 U.S.C. § 112).

Rejections under 35 U.S.C. § 112, first paragraph

Claims 1, 13, 14, and 20 are rejected as failing to comply with the written description requirement. In particular, Examiner avers that the terms "completion lines" and "completion descriptors" are "non-descriptive materials."

Applicant respectfully points out that the instant application describes the completion lines at length, including three different types of completion lines (see page 8-9, ll. 9-15 and Fig. 2B of the instant application). Applicant also respectfully points out that the term "completion descriptor" is also defined in the specification as *"configured to describe the packet (e.g., storage location, size, type) so that the host device could retrieve and process it"* (see page 3, ll. 6-11 of the instant application).

Accordingly, Applicant has amended claims 1, 13, 14, and 20 to include the definitions of the three types of completion lines, including completion line of type II, completion line of type I, and completion line of type 0. In addition, Applicant has also explained that the completion descriptor is configured to identify the hybrid buffer in which the completion lines were stored. These amendments find support in page 8, ll. 9- page 9, ll. 19 and page 3, ll. 6-8 of the instant application. No new matter has been added.

Rejections under 35 U.S.C. § 112, second paragraph

Claims 1, 13, 14, and 20 are rejected as being indefinite. In particular, claims 1, 13, and 14 do not include the second payload buffer and hybrid buffer and claim 20 recites the hybrid buffer but claims 1-19 do not. Applicant respectfully submits that the dependent claims of claim 1, 13, and 14 do include a second payload buffer. Applicant has also amended claims 1, 13, and 14 to include the hybrid buffer recited in claim 20. These amendments find support in page 2, ll. 14-23 of the instant application. No new matter has been added.

Claim Objections

Claims 1, 13, 14 and 20 are objected to as being in improper dependent form. In particular, Examiner points out that: (1) claims 1 and 13 recite "the first set or packet (without any comparison to the second set) and null packet;" (2) claim 14 recites "the location and length of the header and payload which are well-known in the art;" and (3) claim 20 details the hybrid buffer.

Applicant respectfully points out that claims 1 and 13 recite a "first subset of the packets" to correspond to the "second subset of the packets" recited in claims 2 and 14. Applicant has amended claims 1 and 13 to remove the phrase "first" in front of the phrase "buffer". Applicant has also amended claims 1, 13, and 14 to include a hybrid buffer recited in claim 20. These amendments find support in page 2, ll. 14-23 of the instant application. No new matter has been added.

With respect to the objection to claim 14, Applicant respectfully points out that although the location and length of header and payload are well known in the art, placing such information in a completion line in order to facilitate transferring packet(s) to a host computing device is *not* well known in the art. Applicant has accordingly amended claim 14 to describe in detail the completion lines of type I and 0.

Double Patenting Rejection

Claims 20-26 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 if U.S. Patent No. 6,480,489.

Applicant respectfully submits the attached terminal disclaimer with respect to the above U.S. Patent No. 6,480,489 B1 to obviate any rejection under the judicially created doctrine of obviousness-type double patenting.

Rejections under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a)

Claims 1-19 were rejected as being anticipated by Iyer. Claims 20-26 were rejected as being unpatentable over Iyer in view of Hammond. Applicant respectfully disagrees because Iyer and Hammond do not disclose: (1) using completion lines to facilitate transferring multiple packets to a host computing device, or (2) using a single completion descriptor to signal the transfer of the multiple packets.

Embodiments of the present invention use **completion lines to describe how and where** packets are stored in memory during the transfer (see page 2, ll. 9-13 of the instant application). For example, as shown in FIG. 2A of the instant application, a type II completion line identifies a payload buffer in which payloads of packets may be stored and other information common to the packets, while a type I completion line identifies a length and an offset for each packet including the length and storage location of the header and other information useful for processing the packet, and a type 0 completion line is a null completion line used to indicate that no more packets are currently stored (see page 8, line 9-page 9, line 19 of the instant application).

On the other hand, embodiments of the present invention use a **single completion descriptor** to identify a hybrid buffer in which the completion lines are stored (see page 3, ll. 6-11 of the instant application). In these embodiments, the completion descriptor is released to software, which then accesses the identified hybrid buffer to read the completion lines and retrieve the packets (see page 6, ll. 8-16 of the instant application).

In contrast, Iyer discloses an input/output processor for analyzing and efficiently handling common input/output and memory access patterns (see par. [0013] of Iyer). The input/output processor may offload work from the main process, divide memory storage tasks into components based on frequency and availability, or allocate memory storage task in a manner such that all memory

bank conflicts are eliminated (see pars. [0014]-[0016] of Iyer). Nothing in Iyer discloses: (1) using completion lines to facilitate transferring multiple packets to a host computing device, or (2) using a single completion descriptor to signal the transfer of the multiple packets.

Regarding the Examiner's argument that Iyer discloses a hybrid buffer and pads the remaining with null in paragraph [0312], Applicant respectfully points out that the "hybrid memory" system disclosed in Iyer is different from the "hybrid buffer" in embodiments of the present invention. The hybrid memory in Iyer refers to a memory system that contains both a small amount of high-speed memory and a larger low-speed memory (see par. [0310] of Iyer). In contrast, the hybrid buffer in the embodiments of the present invention refers to a buffer that stores small packets and completion lines and optionally the packet's header (see page 7, ll. 7-13 of the instant application). In addition, Iyer's "padding the remaining null" is different from writing a null completion line as in the embodiments of the present invention, which indicates no more packets are currently stored (see page 2, ll. 26-27 of the instant application).

On the other hand, Hammond discloses a processor having two system configurations (see col. 2, ll. 15-33 of Hammond). Handlers and interruption descriptors are used to deliver an event (see col. 8-9, ll. 55-12 of Hammond). Nothing in Hammond discloses: (1) using completion lines to facilitate transferring multiple packets to a host computing device, or (2) using a single completion descriptor to signal the transfer of the multiple packets.

In page 6 of Office Action, Examiner avers that:

> "[I]t would have been obvious to an ordinary skill in the art at the time of invention was made to incorporate the techniques of identify the location of packet payload in the buffer and location of header in the hybrid memory system as taught by Hammond into the Iyer's apparatus in order to utilize the hybrid memory" (see page 6, 4th paragraph of the Office Action).

Applicant respectfully points out that the mere identification of the locations of packet payload in a payload buffer and header in a hybrid memory system is not equivalent to using completion lines to describe how and where packets are stored in memory during the transfer and/or using a single completion descriptor to signal the host computing device to transfer of a set of packets. The completion descriptor is released to the software by changing an ownership indicator or by singling an interrupt, thus only one interrupt is needed for a set of packets (see page 6, ll. 13-16 of the instant application). Using a single completion descriptor enables the embodiments of the present invention to efficiently transfer sets of packets from communication hardware to a host computing device or software (see page 2, ll. 9-13 of the instant application).

Accordingly, Applicant has amended claims 1, 13, 14, and 20 to clarify that embodiments of the present invention use completion lines to indicate the locations of the packet payloads in the memory, and use a single completion descriptor is used to signal the transfer of multiple packets.

Hence, Applicant respectfully submits that independent claims 1, 13, 14, and 20 as presently amended are in condition for allowance. Applicant also submits that claims 2-12, which depend upon claim 1, claims 15-19, which depend upon claim 14, and claims 21-26, which depend upon claim 20, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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Date: 15 November 2007

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